UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,800	11/08/2001	Mark A. Gerber	SC11588TK	7112

23125 7590 11/14/2003

MOTOROLA INC
AUSTIN INTELLECTUAL PROPERTY
LAW SECTION
7700 WEST PARMER LANE MD: TX32/PL02
AUSTIN, TX 78729

EXAMINER	
ROMAN, ANGEL	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 11/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,800	GERBER ET AL.	
	Examiner	Art Unit	
	Angel Roman	2812	

-- Th MAILING DATE of this communication appears on th cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 August 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *16-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 28-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *08042003* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings were received on 08/04/03. These drawings are acceptable.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 30 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Jeng et al. U.S. Patent 6,133,067 A.

Jeng et al. discloses a method for forming a package device, comprising; providing a package substrate 17 having a first surface along a first plane and second surface along a second plane, wherein the package substrate 17 has a cavity between the first plane and the second plane (see figure 3C); placing a first integrated circuit 12 in the cavity; placing a second integrated circuit 11 adjacent to the first integrated circuit 12 outside the cavity, such that a supporting member 13 is interposed between the first integrated circuit 12 and the second integrated circuit 11, and depositing encapsulating material over the first integrated circuit and the second integrated circuit (see figure 3F). Jeng et al. also discloses interposing die attach material between the first integrated circuit and the second integrated circuit (see column 3, lines 21-24).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 1, 6, 7 and 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin et al. U.S. Patent 6,515,356 B1 in view of Lin et al. U.S. Patent 5,273,938 A.

Shin et al. discloses a method for forming, a package device, comprising; providing a package substrate 10 having a first surface along a first plane and second surface along a second plane, wherein the package substrate has a cavity between the first plane and the second plane (see figure 10A); attaching a tape C to the package substrate along the first plane (see figure 10A); placing a first integrated circuit 2 on the tape C and in the cavity (see figure 10C); depositing encapsulating material 20 over the first integrated circuit 2 (see figure 10E); removing the tape C (see figure 10G); placing a second integrated circuit 3 adjacent to the first integrated circuit 2 outside the cavity; and depositing encapsulating material over the second integrated circuit (see figure 6A). The second integrated substrate 3 is placed adjacent to the first integrated substrate 2 outside the cavity, such that no substrate is interposed between the first integrated circuit 2 and the second integrated circuit 3 (see figure 6A). A first portion of the encapsulating material 20 is deposited over the first integrated circuit 2 prior to the step of placing the second integrated circuit 3; and a second portion of encapsulating material is deposited over the second integrated circuit 3. The package substrate further comprises first pads on the first surface, second pads on the second surface, first bond fingers 12 on the first surface, and second bond fingers on the second surface, further comprising; electrically connecting by wire bonding the first integrated circuit to the first pads; and electrically connecting the second integrated circuit to the

second pads (see figure 6A). The supporting member C may comprise an electrically conductive material (see column 10, lines 21-27). The step of depositing the first portion of the encapsulating material 20 comprises transfer molding the encapsulating material (see figure 13).

Shin et al. is applied as above but lacks anticipation on disclosing die attach material interposed between the first integrated circuit and the second integrated circuit. Lin et al. discloses a method of forming a package device using a die attach material 22 interposed between a first integrated circuit and a second integrated circuit; therefore it would have been obvious to a person having ordinary skills in the art at the time the invention was made to use die attach material in the primary reference of Shin et al. as disclosed in Lin et al. since it would provide stability to the second integrated circuit and prevent damage during the encapsulation process.

8. Claims 2-5, 9, 10 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin et al. U.S. Patent 6,515,356 B1 in view of Lin et al. U.S. Patent 5,273,938 A as applied to claims1, 6, 7 and 11-15 above, and further in view of Higgins, III U.S. Patent 5,291,062 A.

Shin et al. in view of Lin et al. is applied as above but lacks anticipation on testing the first integrated circuit and the second integrated circuit by applying test probes to the first pads and the second pads; and disclosing a transfer molding process for encapsulating the second integrated circuit.

With respect to testing the first integrated circuit and the second integrated circuit by applying test probes to the first pads and the second pads, Higgins, III discloses testing an integrated circuit by applying test probes (see column 4, lines 32-40). In view of this disclosure, it would have been obvious to a person having ordinary skills in the art at the time the invention was made to test the integrated circuit in the primary reference of Shin et al. as modified by Lin et al. by applying probes as disclosed in Higgins, III, since unnecessary packaging cost may be prevented by testing the circuit functionality.

Regarding disclosing a transfer molding process for encapsulating the second integrated circuit, it would have been obvious to a person having ordinary skills in the art at the time the invention was made to disclose a transfer molding process for the second integrated circuit 3 in the primary reference of Shin et al. as modified by Lin et al. since Shin et al. is already using a transfer molding process for the first integrated circuit.

9. Claims 8 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin et al. U.S. Patent 6,515,356 B1 in view Lin et al. U.S. Patent 5,273,938 A as applied to claims 1, 6, 7 and 11-15 above, and further in view of Halahan U.S. Patent Application Publication 2003/0047798 A1.

Shin et al. as modified by Lin et al. is applied as above but lacks anticipation on disclosing a third integrated circuit adjacent to the second integrated circuit prior to the step of depositing the second portion of encapsulating material, wherein the third

integrated circuit is stacked at least partially overlying one of the first and second integrated circuits. Halahan discloses stacking a third integrated circuit 104.2 adjacent to a second integrated circuit, wherein the third integrated circuit is stacked at least partially overlying one of a first and second integrated circuits (see figure 1). In view of this disclosure, it would have been obvious to a person having ordinary skills in the art at the time the invention was made to disclose a third integrated circuit adjacent to the second integrated circuit prior to the step of depositing the second portion of encapsulating material, wherein the third integrated circuit is stacked at least partially overlying one of the first and second integrated circuits in the primary reference of Shin et al. as modified by Lin et al. as disclosed in Halahan since it would provide a desire package density.

Response to Arguments

10. Applicant's arguments with respect to claims 1-15, 28 and 29 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yamaguchi et al. and Asada disclose methods for forming package devices by encapsulating semiconductor devices and stacking the semiconductor devices after the encapsulation process.

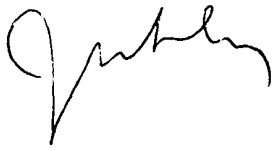
12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel Roman whose telephone number is (703) 306-0207. The examiner can normally be reached on Monday-Friday 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.



AR
29 October 2003